Galvanic separated I/O Module MOD_013

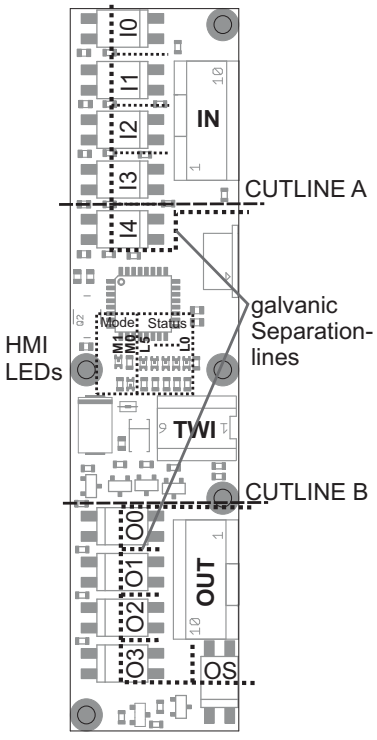
Preliminary

May 29, 2013

1 Features

- Galvanic separated signal handling
- Five independent isolated inputs
- Five independent isolated outputs
- Wide range input/output voltage levels
- TWI-Slave with configurable address
- HMI transmitter
- HMI LEDs
- Security output
- Analog- and digital inputs (AC and DC!)

2 Brief Description

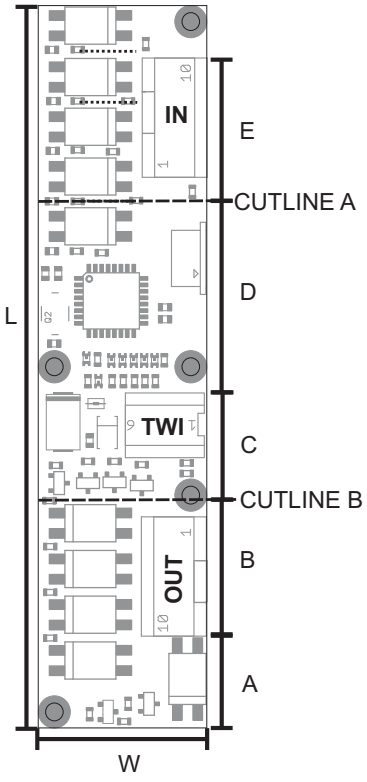


1: MOD_013 Overview

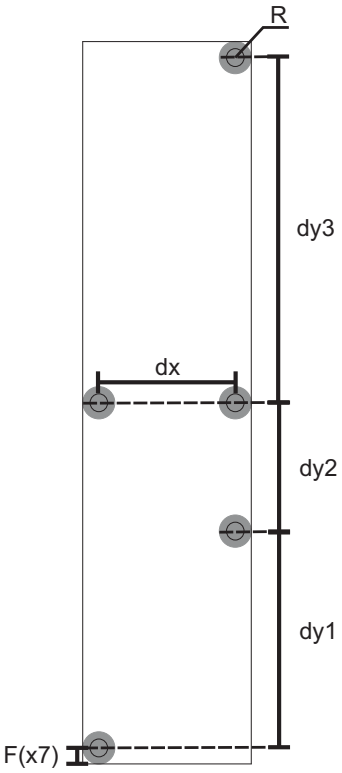
Galvanic isolated signal acquisition and transmission is useful for safety reasons and in applications with floating or large electrical potential differences.
The MOD_013 is the answer for such tasks in the standard Modularis family, directly showing its input and output states with onboard LEDs.
A MOD_013 application example would be the addition of a push button to start and stop a combustion engine equipped with a standard ignition lock. The lock is activated and deactivated by appropriate board output signals and by using the charge control as a feedback signal measured by an input, a controlled start sequence of the engine may be performed. The MOD_013 ensures that these additional signals are isolated from existing electrical systems for safety and reliability reasons.
For additional reliability, one output is designed with a double protection feature to reduce the risk of activation by software faults. For further compactness, the board's inputs or outputs may be removed if desired by cutting the PCB along the indicated lines.

3 Mechanical Dimensions

Symbol	Unit	Value	Description
W	mm	21	width of module
L	mm	90	length of module
A	mm	11.5	distance short edge to OUT connector
B	mm	17.5	distance lower edge of OUT connector to cutline B
C	mm	13	distance cutline B to upper edge of TWI connector
D	mm	23	distance upper edge of TWI connector to cutline A
E	mm	18.5	distance cutline A to upper edge of IN connector
F	mm	2	distance center point of mounting hole to nearest PCB edge
R	mm	1.1	radius of mounting holes, suitable to M2 screw
dx	mm	17	distance between centers of mounting holes in short edge direction
dy1	mm	27	distance dy1 between centers of mounting holes
dy2	mm	16	distance dy2 between centers of mounting holes
dy3	mm	43	distance dy3 between centers of mounting holes



2: Position of Connectors



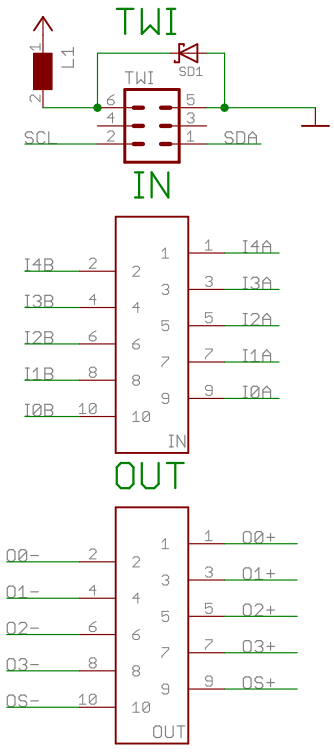
3: Position of Mounting Holes

4 Electrical Specifications

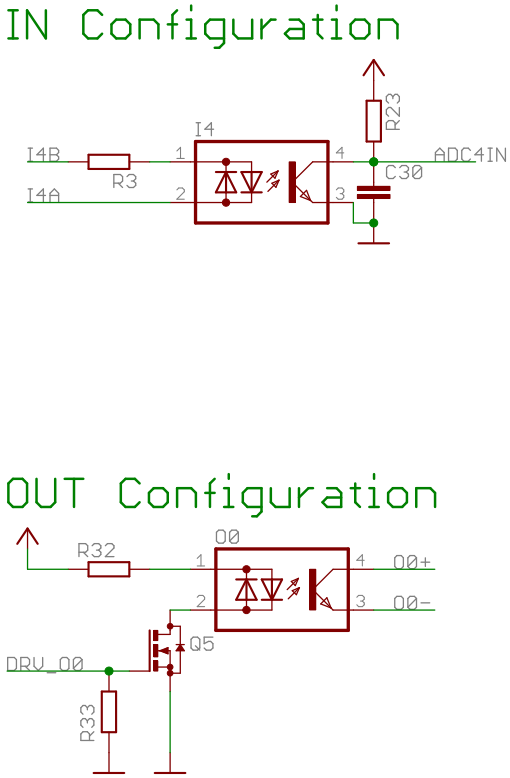
4.1 Schematics

The pin assignments for the MOD_013 TWI, IN and OUT connector are shown in figure 4. All user relevant connectors are Micromatch type. In figure 5 the configuration of standard IN and OUT channels is shown. Note the security out channel (OUTE) also has a high-side switch with a separate control signal for improved security against unintended output activation by software or certain hardware faults.

Symbol	Unit	Value	Description
min. U_{in}	V	2.7	minimum detectable input voltage
max. U_{in}	V	45	maximum input voltage (DC or RMS)
R_{in}	kΩ	47	input resistor ±1% and 0,1 W dissipation rating
f_0	Hz	160	Input 3dB bandwidth
f_u	Hz	1000	Input update rate
max. U_{out}	V	45	maximum output voltage
min. I_{sink}	mA	3	minimal current sink capability of the saturated[1] output transistor
max. I_{sink}	mA	10	maximal current sink capability of the saturated output transistor



4: Pinout of connectors

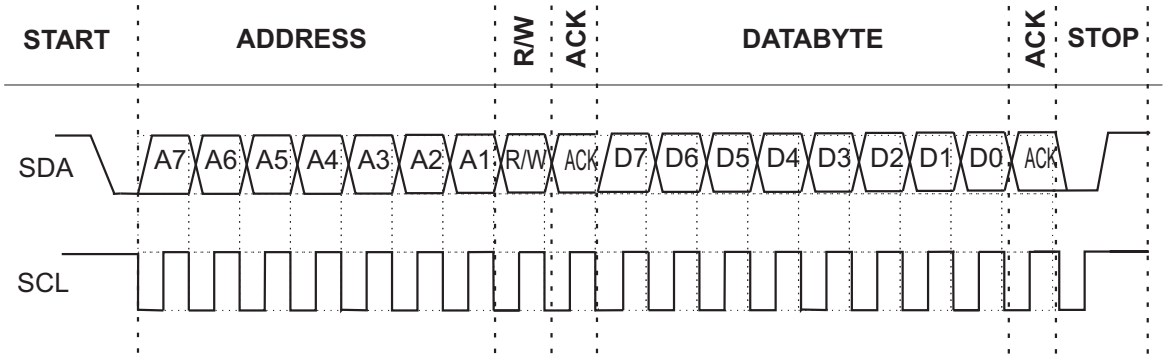


5: Optocoupler configuration

[1] V_{CE} greater than 0.7 Volt

5 TWI Operation and Modularis Protocol

The Modularis Communications Protocol is based on the TWI. In figure 6 a TWI transmission of one byte is illustrated on the physical layer. In figure 7 the same transmission is again illustrated in



6: Typical 1 Byte Transmission Example of Two Wire Interface

an abstract way, such that only the names of the communication sections (Start, Address, Read not Write bit (R/W) and Stop) are sequenced. The Modularis Protocol enables access to the Modularis

START	ADDRESS	R/W	ACK	DATABYTE	ACK	STOP

7: Sections of a simple one Byte TWI Transmission

Slave Devices' 16-bit register structure. Each element of this structure is indexed by an 8-bit value - therefore the structure is limited to 256 registers in first order. A write access consists of three transmitted bytes. The first byte denotes the index of the register to be written to. The trailing two bytes represent the data to be written to the register. The Modularis Register write sequence is illustrated in figure 8. Reading from any register consists of an one byte write access to setup the

START	ADDRESS	W	ACK	INDEX	ACK	MSByte	ACK	LSByte	ACK	STOP

8: Modularis TWI protocol write sequence

index register. After this the index points to the register of interest. This means that any future read access will deliver the two bytes representing the current state of the register, which could represent a volatile sensor value.

START	ADDRESS	W	ACK	INDEX	ACK	STOP

START	ADDRESS	R	ACK	MSByte	ACK	LSByte	ACK	STOP

9: Modularis TWI protocol read sequence

6 Registers

Index	Registername	Memo	R/W	Unit	min.	typ.	max.
0	Binary Input Register	BIR	R	-	0	31	31
1	Binary Output Register	BOR	R/W	-	0	31	31
2	Security Output Register	OSR	R/W	-	0	0	31
3	Digital Comparator Level	DCL	R/W	-	10	100	1000
11	Analog Channels 0 and 1	A0A1	R	-	0	-	65536
12	Analog Channels 2 and 3	A2A3	R	-	0	-	65536
13	Analog Channel 4	A4	R	-	0	-	255
16	Current Slave Address	CSA	R	-	0	5	31
17	Intended Slave Address 1	ISA1	R/W	-	0	5	31
18	Intended Slave Address 2	ISA2	R/W	-	0	5	31
32	Set Intended Address	SIA	R/W	-	0	0	65536

6.1 Binary Input Register BIR

Bit Nr.°	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bit Name	–	–	–	–	–	–	–	–	–	–	–	I4	I3	I2	I1	I0

An analog digital converter samples the the inputs I0 - I4 at a minimum of 1 kHz. The result is compared to the DCL register, if it is greater the corresponding Bit in the binary input register is set. Zero voltage at the input means a zero in the corresponding bit.

6.2 Binary Output Register BOR

Bit Nr.°	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bit Name	–	–	–	–	–	–	–	–	–	–	–	OS	O3	O2	O1	O0

Writing to the Binary Output Register (BOR) directly affects the status of the outputs. For example, a '0' in Bit O0 causes the optocoupler to behave like a closed switch and a '1' causes an open switch behavior. Note, that the security output OS is only affected if the output security register (OSR) is written with an appropriate keyword.

6.3 Output Security Register OSR

To change the status of the security output OS, the Output Security Register must be set to the bitwise complement of the BOR register. Otherwise, the status of the OS output is not affected.

6.4 Digital Comparator LEVEL (DCL) and Analog Channels (AxAy)

Every input is sampled with a 10-bit ADC. The most significant eight bits of the 10-bit ADC result are transferred to the corresponding byte in the corresponding register AxAy.

6.5 Current Slave Address (CSA), Intended Slave Address (ISA) 1 and 2

Bit Nr.°	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Bit Name	–	–	–	–	–	–	–	–	–	A6	A5	A4	A3	A2	A1	A0

There are three registers providing control of the device's slave address. The Current Slave Address (CSA) reflects the current slave address on the TWI bus. The two Intended Slave Address (ISA) Registers can be set by the user. They have to agree for a change of address to occur. The change is made when the keyword consisting of the current slave address (most significant byte) and intended slave address (least significant byte) is written to the Set Intended Address (SIA) register. Note the device will keep its last slave address in a static memory.

7 HMI LEDs

On the MOD 013, seven LEDs (one blue, one red, and five green) display the slave address and the digital input and output states. The blue and red LEDs indicate the type of message mode that is encoded & displayed by the five green LEDs. At power up and after changing the I2C address of the device, the module displays the current adress for three seconds. Otherwise the Mode toggles between Current Input State and Current Output State. For this reason, the LEDs M0 and M1 are not placed in line but on respective input and output sides of the board.

Display	LED M1	LED M0	LED L4	LED L3	LED L2	LED L1	LED L0
	blue	red	green	green	green	green	green
Current I2C Address	1	1	A4	A3	A2	A1	A0
Current Input State	1	0	I4	I3	I2	I1	I0
Current Output State	0	1	OS	O3	O2	O1	O0
Reserved	0	0	-	-	-	-	-

8 Coming soon

The register structure presented here will be rapidly extended to include the following functionality

- Modularis Software concept support
- Watchdog functionality
- calibrated linearized ADC functionality
- frequency and amplitude analysis of AC signals
- PWM analysis of AC signals
- PWM output capability
- power save functionalities